

**ARTICLE**

Attempting Doping Activation via Rapid Thermal Annealing in As-Doped Polycrystalline CdSeTe Solar Cells

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ABSTRACT: Doping the absorber layer is a critical process for enhancing the performance of polycrystalline CdSeTe solar cells. Replacing traditional Cu doping with Group V dopants offers a pathway to fabricate devices with improved efficiency and stability. However, the dopant activation rate in polycrystalline structures remains low, typically only a few percent. While rapid thermal annealing (RTA) has been successfully employed to achieve high activation rates in single-crystal CdTe devices, its application to polycrystalline CdSeTe solar cells has been scarcely reported. In this study, we systematically applied multi-step annealing to investigate the dopant activation of *in-situ* As-doped polycrystalline CdSeTe devices. Our findings reveal that polycrystalline devices exhibit significantly lower thermal tolerance than their single-crystal counterparts, sustaining only short-duration annealing at 500°C. Furthermore, although Cl diffusion during RTA can degrade device performance, we observed that trace amounts of CdCl₂ vapor can help stabilize device efficiency.

KEYWORDS: CdTe; solar cells; As doping; activation; rapid thermal annealing

1 Introduction

Polycrystalline CdSeTe solar cells have established themselves as a mainstream technology in the thin-film photovoltaic market, benefiting from their low manufacturing cost, structural stability, long operational lifetime, and considerable power conversion efficiency. Notably, First Solar Inc. has achieved a certified efficiency of 23.1% [1]. For many years, Cu has been the conventional dopant for p-type doping in the absorber layer and back contact formation. Although Cu doping is a mature process that substantially enhances device performance [2–4], it also leads to long-term degradation due to the high diffusion coefficient of Cu [5,6]. Moreover, the carrier concentration in Cu-doped devices is generally limited to the order of 10¹⁴ cm⁻³, a consequence of self-compensation effects and grain boundary segregation [7]. The deep transition level of Cu further complicates efficient ionization and can promote carriers recombination, thereby compromising device performance.

In recent years, Group V dopants—such as N, P, As and Sb—have been identified as promising alternatives to Cu [8,9]. These elements exhibit superior doping stability, shallower transition levels, and the potential to achieve higher carrier concentrations [10]. Several studies have reported Group V-doped devices with efficiencies approaching or exceeding 20%, with arsenic (As) being the most commonly employed dopant in this category [11–14].

In successful cases of As doping in polycrystalline CdTe films, carrier concentrations can exceed 10^{16} cm^{-3} , but the dopant activation rate remains low—typically only a few percent [12,15]. In contrast, single-crystal CdTe devices have demonstrated activation efficiencies exceeding 40% [16]. A key reason contributing to this high activation in single-crystal systems is their ability to endure higher annealing temperatures. Both experimental and simulation studies confirm that the activation rate of Group V dopants improves with increasing temperature during RTA [10]. However, in polycrystalline devices—which often involve CdCl_2 treatment during annealing and possess distinct microstructures—excessively rapid CdCl_2 diffusion at elevated temperatures can cause interfacial damage and over-treatment.

Recent research on single-crystal CdTe has shown that As dopant activation can be completed within a short duration, and such devices can withstand multiple annealing cycles, with the final activation rate determined primarily by the temperature of the last annealing step [17]. Inspired by these findings, we hypothesize that a multiple annealing strategy may also be applicable to polycrystalline devices. This approach aims to enhance dopant activation while mitigating the risks of over-treatment associated with rapid CdCl_2 diffusion at high temperatures. To test this, we performed RTA at 500°C or 575°C following a standard chlorine heat treatment (CHT) at 395°C .

In this study, close-space sublimation (CSS) was employed to fabricate As-doped CdSeTe absorber layers, confirming the effectiveness of CSS for As incorporation. By systematically comparing devices subjected to CHT only, RTA only, and combined CHT + RTA treatments, we evaluate the role of RTA in activating As dopants and examine how annealing time and temperature influence device performance. We further demonstrate that a low-concentration CdCl_2 atmosphere during RTA contributes to the stabilization for device performance.

2 Experiment

Fig. 1 shows our device structure. MZO, CdS, and CdSe were sequentially deposited via magnetron sputtering onto fluorine-doped tin oxide glass (TecTM 12D). We found that devices incorporating a thin CdS layer demonstrate better reproducibility. The CdS layer is only 20 nm thick and interdiffuses with CdSe and CdTe during CHT. After CHT, the CdS layer no longer exists near the front interface, so it does not affect the blue response of the cell, as can be seen in the EQE measurements discussed later. The CdTe:As layer was deposited by CSS with a source temperature of 635°C and a substrate temperature of 570°C .

The CdTe:As source containing CdTe and 1 wt.% Cd_3As_2 was obtained by the rotating vertical Bridgman melt growth technique [18]. The devices then underwent optimized CHT: 0.05 mol/L CdCl_2 aqueous solution was uniformly sprayed onto the deposited CdTe:As film surface using an ultrasonic sprayer for 90 s, followed by annealing at 395°C for 40 min. CdSe and CdTe interdiffuse during CHT to form the CdSeTe layer. Samples that have undergone CHT are considered baseline cells. Baseline cells were carefully cleaned to remove CdCl_2 from the back surface. Note that rinsing with deionized water alone still leaves CdCl_2 residue on the back surface; scrubbing with a brush is necessary. Subsequently, baseline cells underwent RTA in a tube furnace at high temperature of 500°C or 575°C for 3 to 10 min, with a fan used to accelerate cooling. To remove the oxide layer, improve contact resistivity, and clean surface contaminants, samples were etched in 0.2% Br-MeOH solution for 5 s, followed by sequential rinsing with methanol, ethanol, and deionized water. Finally, Au was evaporated as the back contact. For convenient measurement, the devices were segmented into small cells with an area of 0.24 cm^2 via laser scribing, and In electrodes were soldered onto the surrounding FTO.

The average As concentration in the absorber layer was measured by inductively coupled plasma-mass spectrometer (ICP-MS). The absorber layer on the glass substrate was dissolved in dilute HNO_3 solution

and diluted to volume. The detection limit of ICP-MS reaches the ppt level, with a detection limit for As of 5×10^{-6} mg/L. The instrument had been calibrated before the test. The average As concentration in the absorber layer was calculated using the following formula:

$$C_{As} = \frac{m_{As} N_A}{M_{As} V_{film}} \quad (1)$$

where C_{As} is the number of As atoms per unit volume in the absorber layer, i.e., the doping concentration; m_{As} is the total mass of As in the film, obtainable by multiplying the mass concentration of As in the solution by the final solution volume V_0 after dilution, where C_0 is measured by ICP-MS; N_A is Avogadro's constant; M_{As} is the molar mass of As; V_{film} is the film volume, equal to the film area S multiplied by the total thickness L ; the film thickness was measured at multiple points using a step profiler, and the average value was taken. The film was assumed to be uniformly thick, and the area was measured up to the point where the film thickness rapidly decreases at the edge. There is some error in the measurement of V_{film} , but it is within an acceptable range.

The carrier concentration of the absorber layer was obtained from capacitance-voltage measurement (C-V) under dark conditions, at a frequency of 100 kHz, a step size of 5 mV, and a bias voltage ranging from -1 V to 1 V. C-V were performed using an Agilent 4156 semiconductor parameter analyzer. Light J-V measurements were performed under standard AM1.5 G illumination (100 mW/cm^2) using a Sun 3000 solar simulator (ABET Technologies). Prior to measurement, the light intensity was precisely calibrated with a NIST-traceable GaAs reference cell. The external quantum efficiency (EQE) was characterized using a QEX10 measurements. Samples were immersed in liquid nitrogen for low-temperature brittle fracture, and the cross-sections were prepared after sputtering with gold. Scanning Electron Microscope (SEM) and Energy Dispersive Spectrometer (EDS) analyses were performed using a ZEISS GeminiSEM 300 with a magnification of 40k \times .

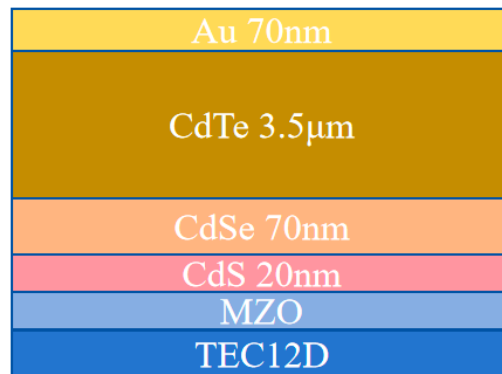


Figure 1: Schematic of the device structure.

3 Results and Discussion

3.1 Verification of CSS Doping Effectiveness

Table 1 shows the As concentration in the digestion solution and the film area and thickness. The total thickness is the sum of the thicknesses of multiple dissolved films. Since the CdTe:As layer is only a few micrometers thick, dissolving too few samples would affect the accuracy of the ICP-MS measurement. Substituting the values from Table 1 into Eq. (1), the As concentration in the CdTe:As layer is $4.18 \times 10^{17} \text{ cm}^{-3}$, which is commonly reported for CSS-fabricated CdSeTe:As or CdTe:As layers [19,20].

According to reported SIMS profiles of As, high concentrations of As segregate at the front interface, which is related to the oxidation of As [21,22]. The actual As concentration in the absorber layer should be less than $4.18 \times 10^{17} \text{ cm}^{-3}$. Fig. 2 shows the efficiency of doped and undoped baseline cells within similar batches, with performance parameters listed in Table 2. The performance of the doped device is significantly improved, especially in terms of Voc and FF. Improvement of hole concentration in the absorber layer can enhance the separation efficiency of photogenerated carriers, reduce non-radiative recombination, and increase Voc. Simultaneously, the increased carrier concentration improves the conductivity of the absorber layer, leading to a reduction in Rs and an increase in FF. As doping greatly improves device performance, demonstrating the effectiveness of *in-situ* As doping via CSS.

Table 1: Parameters of the CSS-deposited CdTe:As layer.

V_0 (mL)	C_0 (ug/L)	S (cm ²)	L (μm)	M_{As}	m_{As} (g)	C_{As} (cm ⁻³)
40	20	15.84	9.7	74.92	8×10^{-7}	4.18×10^{17}

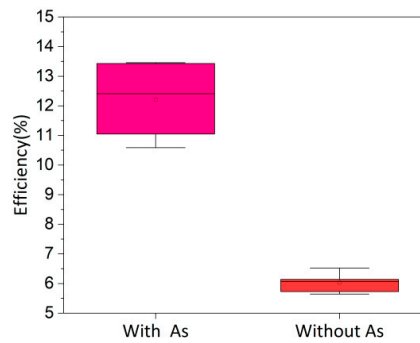


Figure 2: Efficiency of As-doped and undoped devices after CHT.

Table 2: Performance parameters from light J-V curves of As-doped and undoped devices after CHT.

	Eff (%)	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)	R_s (Ω·cm ²)	R_{sh} (Ω·cm ²)
Without As	6.52	25.92	537	46.83	9.41	157.78
With As	13.46	27.53	803	60.84	6.85	749.33

3.2 Activation of As Doping

RTA is widely used for Group V dopant activation in single-crystal CdTe but is rarely applied to polycrystalline CdSeTe activation. Single-crystal CdTe has no grain boundaries, unlike polycrystalline CdSeTe, thereby obviating the need for both CHT and the interdiffusion process between CdSe and CdTe. More importantly, the structure of single-crystal CdTe devices differs from polycrystalline devices; polycrystalline CdSeTe uses a superstrate configuration where the interface forms during absorber layer deposition and persists throughout the annealing process. It is necessary to verify whether RTA can be applied to polycrystalline devices. This study employed two RTA temperatures: 575°C annealing and a milder 500°C annealing. The 575°C RTA temperature has been validated for single-crystal CdTe activation [17].

Due to inherent variations between baseline cells, even under identical preparation condition, the performance of optimized cells might still be lower than the best baseline cell in Fig. 2. In subsequent

experiments, unless otherwise specified, samples within the same figure are derived from portions of the same baseline cell, allowing for comparison based on the performance of that specific baseline cell.

3.2.1 As Activation without CHT

RTA at 500°C without prior CHT is shown in Process ① in Fig. 3. The sample was directly subjected to RTA without undergoing CHT, excluding the influence of CdCl₂. The absorber layer was deposited at 570°C, higher than the RTA temperature of 500°C. However, the CSS system requires the source temperature to be below 200°C when extracting samples from the chamber, forcing the absorber layer to cool slowly within the chamber, so it is anticipated that RTA would also be effective for devices that have not undergone CHT. Fig. 4a shows the light J-V curves of a device without CHT before and after RTA at 500°C for 6 min, with performance parameters listed in Table 3. Device performance improved significantly. This improvement is not attributed to recrystallization or Se diffusion. The absorber layer requires CHT for recrystallization and to assist Se diffusion. Process ① lacks CHT, so there is no Cl-induced recrystallization process. Furthermore, the annealing time (6 min) and temperature (500°C) are significantly lower than the deposition time (30 min) and temperature (575°C). This suggests that the RTA process, being milder and shorter than deposition conditions, has a limited impact on Se diffusion. Fig. 4b shows the C-V measurements of devices without CHT. The upward shift of the C-V curves after RTA reflects an increase in carrier concentration. The carrier concentration increases from $7.2 \times 10^{13} \text{ cm}^{-3}$ to $1.2 \times 10^{14} \text{ cm}^{-3}$. It is inferred that the performance improvement is due to an increased As dopant activation rate induced by RTA. This result indicates that RTA can increase carrier concentration without CHT, consistent with the trend observed in single-crystal CdTe. Based on the property that dopant activation rates in CdTe and CdSeTe improve with increasing temperature [10], the activation effect at 575°C should be more pronounced than at 500°C. The C-V for devices annealed at 575°C is not presented here because annealing at excessively high temperatures can induce effects beyond increased carrier concentration, which may interfere with C-V measurements and obscure the true carrier concentration, as detailed later. Note that heating via a tube furnace requires a certain amount of time. If the annealing time is too short, the temperature achievable by the absorber layer may be insufficient to induce dopant activation.

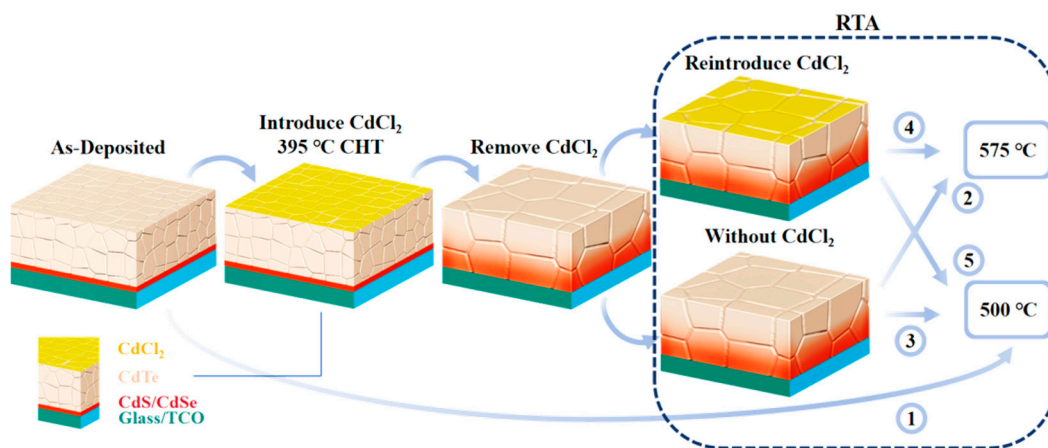


Figure 3: Schematic diagram of CHT and RTA processes.

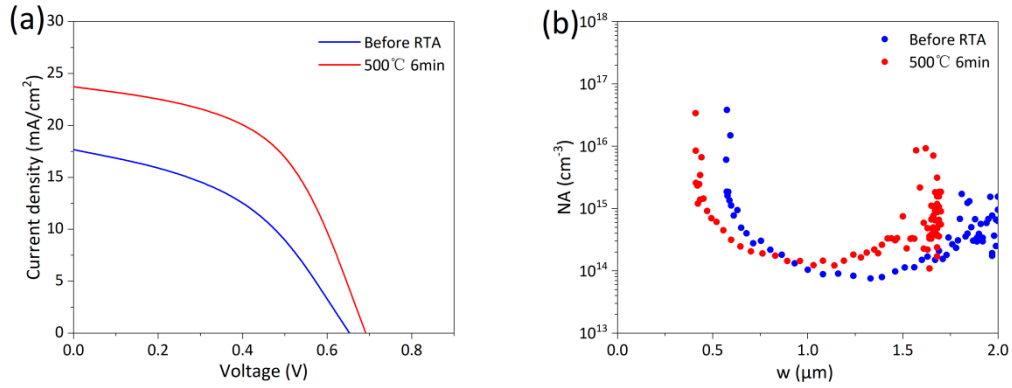


Figure 4: (a) Light J-V curves of devices without CHT before and after RTA. (b) C-V measurements of devices without CHT before and after RTA.

Table 3: Performance parameters from light J-V curves of devices without CHT before and after RTA.

	<i>Eff</i> (%)	<i>Jsc</i> (mA/cm ²)	<i>Voc</i> (mV)	<i>FF</i> (%)	<i>Rs</i> (Ω·cm ²)	<i>Rsh</i> (Ω·cm ²)
Before RTA	5.03	17.67	653	43.57	16.09	122.99
500°C 6 min	8.54	23.73	691	52.05	9.14	187.28

3.2.2 As Activation after CHT

Baseline cells were activated by RTA at 575°C for 10 min, as shown in Process ② in Fig. 3. This condition has been validated for single-crystal device activation [17]. Fig. 5a,b shows the J-V and EQE curves before and after activation, respectively, with performance parameters listed in Table 4. Device efficiency decreased significantly after RTA and the EQE response also degraded. No obvious changes were observed visually from the glass side before and after RTA, but oxidation traces were present on the back surface of the absorber layer, analyzed in detail later. Clearly, polycrystalline CdSeTe devices have much lower tolerance to high temperatures compared to single-crystal CdTe devices, which can be rapidly cooled from temperatures close to 1000°C [16,23]. Activation rate is positively correlated with annealing temperature, making As activation more challenging in polycrystalline CdSeTe than in single-crystal CdTe. Simply applying single-crystal activation conditions to polycrystalline devices is not advisable.

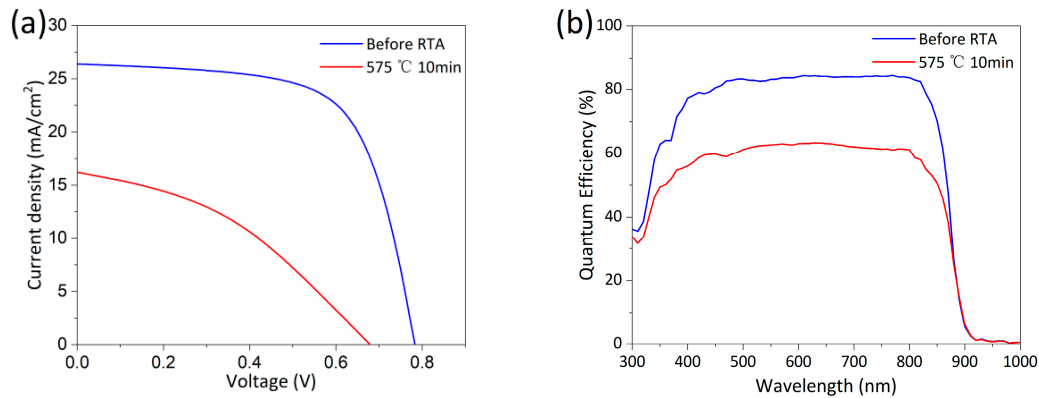


Figure 5: (a) Light J-V curves of baseline cells before and after RTA at 575°C for 10 min. (b) EQE curves of baseline cells before and after RTA at 575°C for 10 min.

Table 4: Performance parameters from light J-V curves of baseline cells before and after RTA at 575°C for 10 min.

	<i>Eff</i> (%)	<i>J</i> _{sc} (mA/cm ²)	<i>V</i> _{oc} (mV)	<i>FF</i> (%)	<i>R</i> _s (Ω·cm ²)	<i>R</i> _{sh} (Ω·cm ²)
Before RTA	13.57	26.40	783	65.65	4.66	606.93
575°C 10 min	4.25	16.21	679	38.55	24.26	127.69

Baseline cells were activated by RTA at 500°C, as shown in Process ③ in Fig. 3. Fig. 6a shows the light J-V curves of devices with different annealing times, and their performance parameters are listed in Table 5. Compared with the baseline cell, the efficiency of activated cells changed little within 3 min, likely because the absorber layer reaches a limited temperature when the annealing time is short. Efficiency slightly decreased for the 5 min device and significantly decreased for the 10 min device, though it remained higher than the sample annealed at 575°C from Fig. 5a. Fig. 6b shows the EQE curves of devices with different annealing times. The EQE curves show little difference up to 5 min but decreased significantly at 10 min, especially in the short-wavelength range. Fig. 6d shows the C-V measurements of samples annealed for up to 5 min. A significant increase in carrier concentration, from $8.4 \times 10^{13} \text{ cm}^{-3}$ to $2.5 \times 10^{14} \text{ cm}^{-3}$, is observed after just 5 min of RTA. This result demonstrates that RTA rapidly activates doping in samples that have undergone CHT, a finding consistent with literature reports [17]. It also confirms the limited influence of Cl on the doping activation process. The C-V curves of the sample after 3 min of RTA is basically consistent with that of the base cell, which once again demonstrates that if the RTA time is too short, the actual temperature reached by the sample is insufficient to activate doping. It also verifies that the C-V curves of samples from the same base cell exhibit good consistency. This experiment, together with the experiment without CHT in Fig. 4b, demonstrates that RTA can increase carrier concentration for cells both with and without prior CHT. However, although carrier concentration increased after RTA, device efficiency decreased. This suggests that other phenomena occur concurrently with RTA and negatively impact the device, and this effect should be related to Cl diffusion, as discussed in detail in the following. Note that after annealing at 500°C for 10 min, no significant difference was observed at the front interface, while oxidation traces were present on the back surface, which darkened in color. Oxides are predominantly CdTeO₃, commonly found under annealing conditions above 450°C [24]. CdTeO_x phases were also observed in our previous air-annealed samples [25]. However, the RTA-treated samples showed more pronounced oxidation traces. This enhanced oxidation occurred because the RTA was performed in unsealed air (without degassing) to facilitate rapid sample extraction from the tube furnace for cooling, thereby exposing the samples to more oxygen. All samples in Fig. 6a were etched with Br-MeOH solution before Au deposition to remove the back surface oxide. To further exclude the influence of the back surface oxide on device performance, we placed the 500°C RTA before CHT without performing etching to remove the back surface oxide layer. Fig. 6c shows the light J-V curve of this sample. Its efficiency is comparable to or even higher than the baseline cell efficiency. Some studies have shown that the surface oxides formed after prolonged low-temperature annealing may actually enhance device performance, which is inconsistent with the phenomenon we observed [26]. This indicates that the presence of the back surface oxide is not the main factor causing device efficiency degradation. Interface damage at high temperatures or Cl diffusion from the front interface and grain boundaries into the grain interiors during RTA are considered the primary suspects for the performance loss.

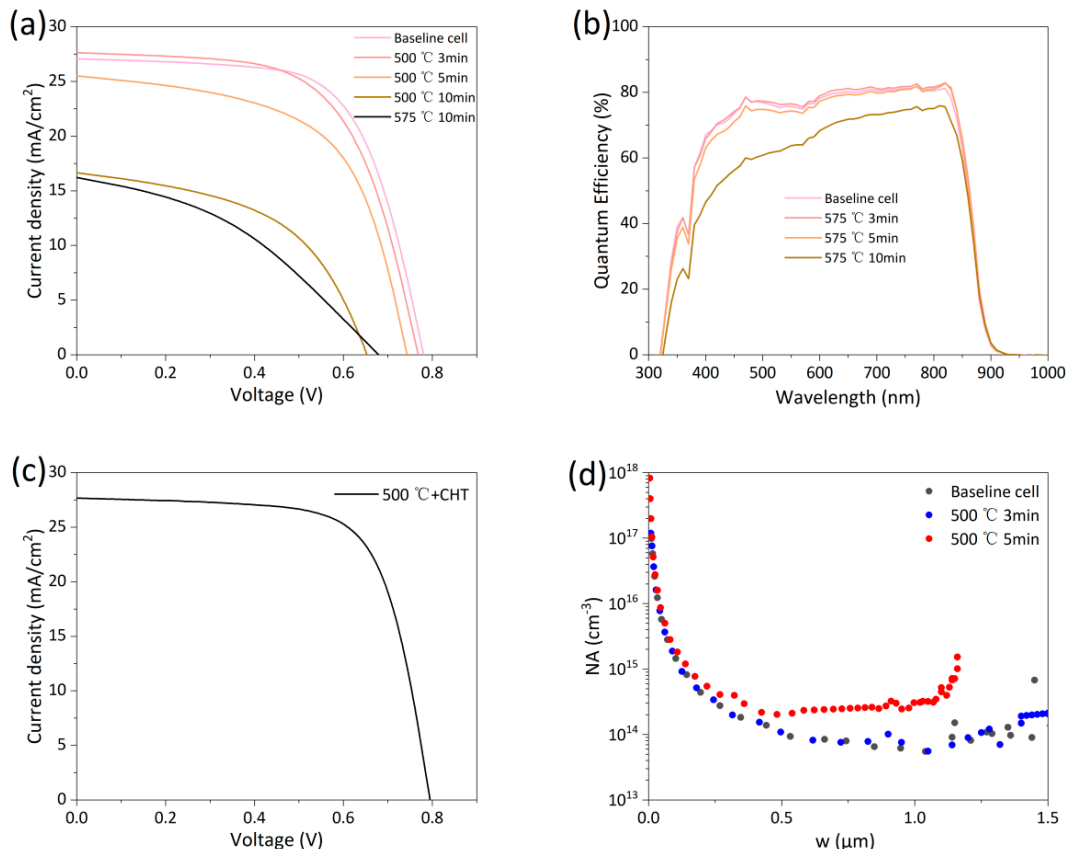


Figure 6: (a) Light J-V curves of baseline cells after RTA at 500°C for different times. (b) EQE curves of baseline cells after RTA at 500°C for different times. (c) Light J-V curve of devices subjected to 500°C, 10 min RTA first, followed by CHT. (d) C-V measurements of baseline cells after RTA at 500°C for up to 5 min.

Table 5: Performance parameters from light J-V curves of baseline cells after RTA at 500°C for different times.

	<i>Eff</i> (%)	<i>Jsc</i> (mA/cm ²)	<i>Voc</i> (mV)	<i>FF</i> (%)	<i>Rs</i> (Ω·cm ²)	<i>Rsh</i> (Ω·cm ²)
Baseline cell	13.73	27.07	781	64.96	5.28	787.02
500°C 3 min	13.10	27.63	768	61.68	5.59	666.98
500°C 5 min	11.08	25.51	743	58.45	5.38	243.08
500°C 10 min	5.49	16.65	654	50.40	10.44	186.86

Fig. 7a–d shows cross-sectional SEM images of the FTO/absorber interface for the baseline cell and samples before and after RTA at 500°C from Fig. 6a. No obvious differences were observed between absorber and FTO, consistent with visual inspection. This observation differs from the phenomenon of interface separation caused by excessive grain growth reported in the literature [27]. It is easily explained: typically, grain recrystallization and growth occur during CHT, where CdCl₂ acts as a flux and is continuously replenished. During RTA, even at elevated temperature, the residual CdCl₂ in the absorber layer is insufficient to support significant grain growth. Previous work reported that upon secondary annealing in a CdCl₂-free atmosphere, Cl is removed from the grain boundaries and interiors, thereby becoming undetectable via EDS. This depletion, which in turn facilitates the reappearance of stacking faults, ultimately leads to a significant degradation in device performance [28]. However, comparing the cross-sectional EDS line scans of the various samples from Fig. 6a shown in Fig. 7e, we found that the Cl concentration did

not change significantly after RTA for different times. Fig. 7f shows cross-sectional EDS mapping. The maps for different devices show no obvious differences, and Cl EDS signals persist even after annealing in a CdCl_2 -free atmosphere. This suggests the possibility that Cl diffuses from grain boundaries and the front interface into the grain interiors. Since the volume occupied by grain interiors is much larger than that of grain boundaries and interfaces, even complete diffusion would only marginally increase the Cl concentration within the grains, consistent with the EDS measurement results. CdCl_2 can passivate grain boundaries and interface defects and eliminate stacking faults. Studies show that Cl can occupy up to 25% of Te sites when saturated at grain boundaries [29], and a two-dimensional CdCl_2 layer exists at the front interface [30]. High-efficiency devices should maintain Cl saturation at grain boundaries and interface. During RTA, Cl diffuses into the grain interiors without replenishment from the ambient CdCl_2 atmosphere, potentially leading to insufficient Cl content at grain boundaries or the front interface, causing device performance degradation.

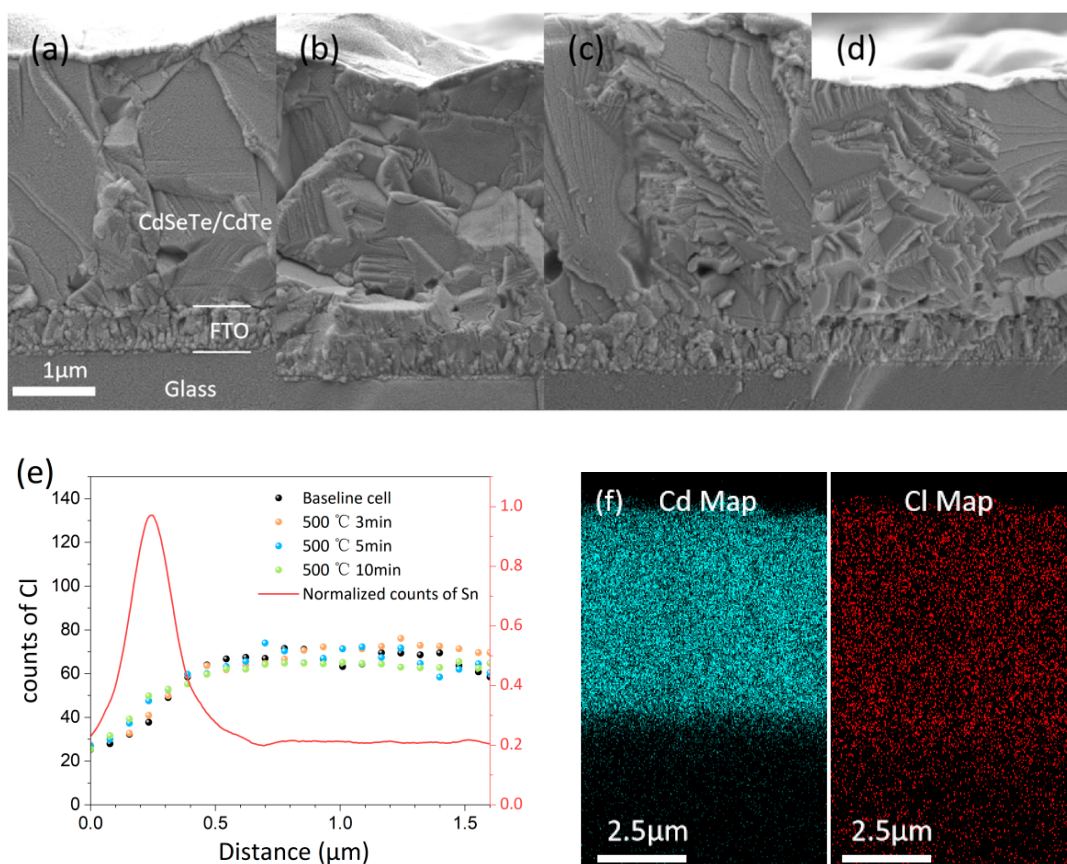


Figure 7: (a–d) Cross-sectional SEM images of the baseline, 3 min, 5 min, and 10 min samples from Fig. 6a, respectively. (e) Smoothed cross-sectional EDS line scans, calibrated by aligning the Sn peak positions. The red line shows the normalized Sn EDS line scan. (f) Cross-sectional EDS maps for Cd and Cl, showing little variation between samples.

Literature reports that devices subjected to secondary annealing in a CdCl_2 -free atmosphere can recover their original efficiency after undergoing CHT again [28]. However, to maintain dopant activation, CdCl_2 vapor must be appropriately retained at high temperatures. Baseline cells were sprayed with a small amount of CdCl_2 aqueous solution followed by RTA at 575 °C, as shown in Process ④ in Fig. 3. The CdCl_2 solution concentration used was 20 g/L, with spray durations of 20 s or 40 s. Fig. 8a shows the light

J-V curves of devices subjected to Process ④, with performance parameters listed in Table 6. All devices after RTA showed significant performance degradation compared to the baseline cell, consistent with the performance change observed in Fig. 5a without CdCl₂ atmosphere. However, the device efficiency was higher when a 20 s CdCl₂ spray was applied compared with no CdCl₂ atmosphere. Note that the baseline cells underwent optimized CHT. Extending CHT time leads to over-treatment and performance degradation, indicating the baseline cells were already fully chlorine-treated. The improvement in device performance with CdCl₂ during RTA suggests that the Cl content in the cell has not reached the optimal concentration, supporting the hypothesis of Cl diffusion from the front interface or grain boundaries. Fig. 8b shows the EQE of the devices from Fig. 8a. When RTA was performed at 575°C, the device EQE decreased, especially in the short-wavelength range. The effect often occurs in insufficiently annealed devices, indicating severe front interface recombination. EQE shows some improvement under an appropriate amount of CdCl₂ vapor during RTA. The performance of the device sprayed with CdCl₂ for 20 s did not recover to baseline cell efficiency as reported in literature, possibly due to insufficient CdCl₂. However, when the CdCl₂ spray time was extended to 40 s, efficiency decreased again, with signs of over-treatment appearing at the front interface. Even with a 40 s spray time during RTA, the amount of CdCl₂ accumulated on the back surface is only about 18% of that under the standard 395°C CHT condition, yet it significantly impacted device performance in a short time. The excessively high diffusion rate of Cl at high temperatures is a major reason for the renewed performance degradation. The difficulty in controlling CdCl₂ diffusion rate at high temperatures led us to adopt a two-step annealing process rather than a single high-temperature CHT step, allowing us to study the impact of RTA on cell performance after the Cl content in the baseline cell reached its optimal concentration. Baseline cells were sprayed with CdCl₂ solution for 40 s and then subjected to milder RTA at 500°C, as shown in Process ⑤ in Fig. 3. Based on Fig. 6a, polycrystalline CdTe devices tolerate RTA well for up to 5 min, so the time was set within 5 min. Their light J-V curves are shown in Fig. 8c and performance parameters are listed in Table 7. Compared to RTA without CdCl₂, device efficiency increased after 500°C annealing. Fig. 8d shows the EQE of samples from Fig. 8c, which remained essentially unchanged before and after RTA. A low-concentration CdCl₂ atmosphere during RTA can stabilize the device's current. The increase in Voc should be attributed to As activation; only when other device performance parameters do not degrade can the increased carrier concentration from As activation lead to an improved Voc. The performance of the 3 min sample is lower than the 5 min sample because the shorter annealing time results in a lower achievable temperature, leading to less pronounced As activation. The reason for the lower device efficiency in Fig. 8c is the lower efficiency of the baseline cell. Typically, we would select groups with higher baseline cell efficiency for analysis. However, the RTA process in a CdCl₂ atmosphere is difficult to control, and only a few groups avoided over-treatment. Even so, the performance change trend of the samples in Fig. 8c after RTA is significantly different from that of samples under other RTA conditions, so the comparison between them is still valuable for analysis.

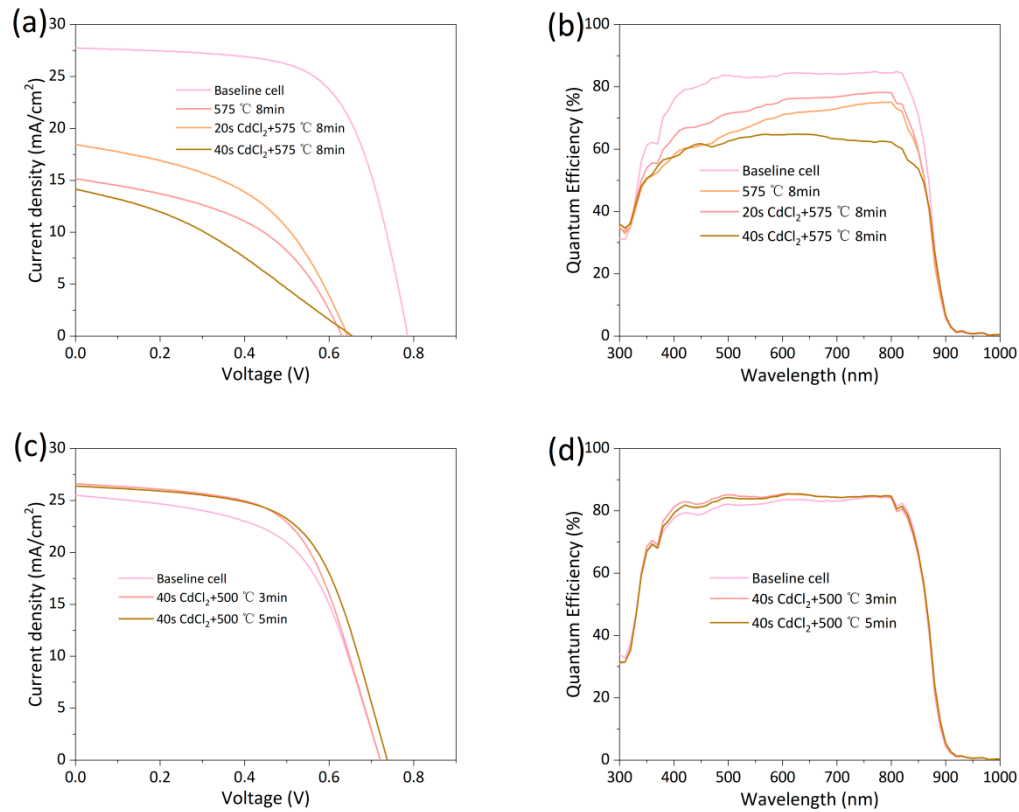


Figure 8: (a) Light J-V curves of baseline cells exposed to 0 s/20 s/40 s CdCl₂ spray before and after RTA at 575°C for 8 min. (b) EQE curves of baseline cells exposed to 0 s/20 s/40 s CdCl₂ spray before and after RTA at 575°C for 8 min. (c) Light J-V curves of baseline cells exposed to 0 s/40 s CdCl₂ spray before and after RTA at 500°C for different times. (d) EQE curves of baseline cells exposed to 0 s/40 s CdCl₂ spray before and after RTA at 500°C for different times.

Table 6: Performance parameters from light J-V curves of baseline cells exposed to 0 s/20 s/40 s CdCl₂ spray before and after RTA at 575°C for 8 min.

	<i>Eff</i> (%)	<i>J</i> _{sc} (mA/cm ²)	<i>V</i> _{oc} (mV)	<i>FF</i> (%)	<i>R</i> _s (Ω·cm ²)	<i>R</i> _{sh} (Ω·cm ²)
Baseline cell	14.26	27.74	787	65.32	5.01	796.96
575 °C 8 min	4.47	15.16	632	46.69	12.70	151.03
20 s CdCl ₂ + 575°C 8 min	5.63	18.45	645	58.45	11.59	143.71
40 s CdCl ₂ + 575°C 8 min	3.12	14.16	648	34.02	32.38	105.06

Table 7: Performance parameters from light J-V curves of baseline cells exposed to 0 s/40 s CdCl₂ spray before and after RTA at 500°C for different times.

	<i>Eff</i> (%)	<i>J</i> _{sc} (mA/cm ²)	<i>V</i> _{oc} (mV)	<i>FF</i> (%)	<i>R</i> _s (Ω·cm ²)	<i>R</i> _{sh} (Ω·cm ²)
Baseline cell	10.51	25.05	721	57.15	7.52	260.03
40 s CdCl ₂ + 500°C 3 min	11.48	26.61	721	59.83	7.32	412.93
40 s CdCl ₂ + 500°C 5 min	11.78	26.39	738	60.53	6.83	454.27

4 Summary

This study utilized CSS evaporation of a CdTe:As source to achieve *in-situ* As doping, which led to a significant efficiency enhancement compared to undoped devices. To prevent over-treatment typically induced by high-temperature CHT, RTA was applied to chlorine-treated baseline cells to activate the As dopants. The results indicate that RTA effectively activates As in devices regardless of prior CHT, and that this activation can be completed within a short time. The oxide layer formed on the back surface during RTA was found to have no significant impact on device performance.

Interface characterization revealed that at high temperatures, the residual CdCl₂ within the absorber layer is insufficient to promote grain growth to an extent that would separate the FTO and absorber layer. However, Cl diffusion from grain boundaries and the front interface was observed to considerably degrade device efficiency. It was also demonstrated that introducing a trace amount of CdCl₂ vapor during RTA plays a stabilizing role in maintaining device performance.

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Abbreviations

The following abbreviations are used in this manuscript:

RTA	Rapid thermal annealing
As	Arsenic
CHT	Chlorine heat treatment
CSS	Close-space sublimation
J-V	Current density–voltage
EQE	External quantum efficiency

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